REMARKS

This paper is responsive to the Non-Final Office Action dated January 4, 2006. Claims 1-58 were examined. Claims 1, 24-26, 45-50, 56-58 were rejected, and the remaining claims were indicated as allowable if rewritten in independent form.

Claim Rejections - 35 U.S.C. § 102

Claims 1, 24-26, 45-50, 56-58 stand rejected under 35 U.S.C. § 102(b) as being anticipated by Winters (U.S. Patent No. 5,515,310). Applicant respectfully traverses this rejection.

Regarding independent claims 1 and 24, the Examiner has cited Winters in Fig. 3 and at column 4, lines 17-67, and more specifically at lines 40-57, in support of the assertion that Winters discloses a circuit comprising "first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices." Applicant respectfully submits that nowhere does Winters teach that such matched devices are susceptible to an *accumulated data-dependent* post-manufacture *shift* in a characteristic of one or more of the matched devices. Applicant respectfully submits that, at best, the Examiner's argument either must find support in an inherency basis, or not at all. Since not all types of transistors fabricated using all generations and variations of semiconductor processes are *necessarily* susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, and absent any teaching of such susceptibility, Applicant respectfully submits that Winters does not teach or suggest such susceptibility.

The Examiner has also cited Winters at column 6, lines 25-34 in support of the assertion that Winters discloses "a preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to cause an initial shift in the characteristic in each of the matched devices and to thereby reduce an expected magnitude of any further lifetime shift in the characteristic of either matched device." This cited text, which is a portion of Winter's claim 1, recites:

a. means for preconditioning the column input and the column-not input to a predetermined logic state thereby forming a preconditioned column input and a preconditioned column-not input wherein the column and column-not lines have opposite logic states one from the other;

b. means for coupling the preconditioned column input and column-not input to the cell forming a stored memory state voltage;

(column 6, lines 25-34) Applicant respectfully submits that this cited text merely describes a means for biasing *circuit nodes* with a particular *logic state*. Winters uses the word "preconditioning" not unlike the use of "precharging", "presetting", or "biasing" certain nodes at certain logic states (i.e., voltage levels). This passage does not teach or suggest a "preconditioning circuit for subjecting the matched devices to a particular condition for a length of time sufficient to *cause an initial shift* in the characteristic in each of the matched devices and *to thereby reduce* an expected magnitude of *any further lifetime shift* in the characteristic of either matched device" as recited in the claim.

Even if, *arguendo*, Winters can be viewed as inherently disclosing "first and second matched devices which are susceptible to an accumulated data-dependent post-manufacture shift in a characteristic of one or more of the matched devices, said shift giving rise to a mismatch in the characteristic between the matched devices", Applicant submits that Winter's circuitry is clearly disclosed as biasing ("preconditioning") individual ones of a pair of nodes to *opposite* logic states in order to write data into a memory cell (i.e., "forming a stored memory state voltage"). Such operation seems to *reinforce* a data-dependent bias being placed across the matched devices. This biasing seems in contradiction to, and would not seem to be capable of, "subjecting the matched devices to a particular condition for a length of time" as recited in the claim.

Regarding independent claim 1, Applicant respectfully submits that Winters provides no teaching or even suggestion of any "preconditioning" step as recited in the claim, with or without use of any preconditioning circuit.

Regarding independent claims 48 and 56, the Examiner's rejection includes the same arguments as the rejection of claims 1 and 24. Applicant respectfully traverses this rejection for the same reasons as described above.

In addition, Applicant respectfully traverses a position advanced by the Examiner regarding subject matter allegedly disclosed by Winters that is relevant to certain of the dependent claims. For example, regarding claims 26 and 50, the Examiner cites Figure 3 as disclosing a cross-coupled pair of PMOS transistors. Applicant respectfully submits that the cited transistors 10, 20, 30, and 40 are NMOS transistors. Winters describes his circuit operation by stating:

> Upon activating the Write line 12 by *raising* it to a logic "1", the transistors 10 and 20 provide a low impedance path from the Column line 14 and the Column-Not line 16 to the gates of the transistors. (column 4, lines 45-48, emphasis added)

Such operation cannot be performed by PMOS transistors configured as shown. Winter's Fig. 3 is also drawn using universally recognized schematic symbols for NMOS devices. Moreover, Winters mentions "enhancement mode NMOS transistors" as preferable, and nowhere mentions PMOS transistors.

The rejected dependent claims are believed allowable at least for their dependence from an allowable independent claim.

Allowable Subject Matter

Claims 2-23, 27-44, 51-55 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims. In light of the believed allowability of the remaining claims, these claims remain without amendment.

Summary

Claims 1-58 are in the case. All claims are believed to be allowable over the art of record, and a Notice of Allowance to that effect is respectfully solicited. Nonetheless, if any issues remain that could be more efficiently handled by telephone, the Examiner is requested to call the undersigned at the number listed below.

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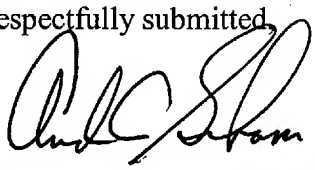
Respectfully submitted,



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